Tutorial 10 Questions

Finite State Machine Design 2

Please try out these self-study questions (labeled "SS"). These will not be discussed in class and solutions will be provided later.

SS1. Implement the circuit of Tutorial 9, Q3 using D flip-flops and minimum logic gates.

SS2. Implement the circuit of Tutorial 9, Q4 using D flip-flops and minimum logic gates.

Q1. A digital circuit is to be designed to implement the "*snooze*" function of an alarm clock. The circuit's input and output signals are as follows:

Inputs: `RING, RESET, CLK`
Output: `ALARM`

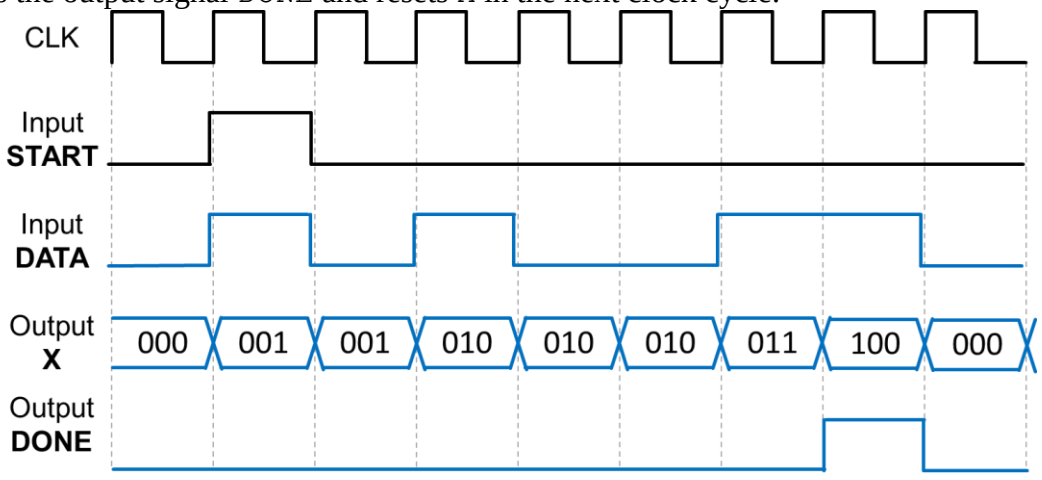
The circuit remains in the "wait" mode until input `RING` is detected to be **TRUE**. When this happens, the circuit goes into the "snooze" mode by ringing the `ALARM` for 10 seconds, waiting for 1 minute and continuously repeats this cycle until the user resets the circuit causing `RESET` to be **TRUE** for one clock period.

Derive the state transition diagram, assuming that an accurate 0.1Hz clock is available as an input. To simplify the state transition diagram, adopt a suitable architectural element as a submachine.

Q2. A digital circuit is designed to find the number of 1's in a serial input `DATA` signal.

Once the input `START` becomes **TRUE**, 7 serial bits are provided consecutively into the circuit via the 1-bit input signal `DATA`, one-bit per clock cycle.

The circuit evaluates `DATA` and continuously updates `X`, a 3-bit output signal. `X` reflects the total number of 1's received up to the current clock cycle. After the 7-bits have been received, the circuit asserts the output signal `DONE` and resets `X` in the next clock cycle.



Derive the state transition diagram for this circuit.

Q3. A synchronous state machine needs to be designed to *count people entering and leaving a room*. The room has a *separate* entrance and exit.

Each door is equipped with a sensor to detect people *coming in through the entrance* or *leaving through the exit*. The sensors provide signals `ENTER` (when a person enters) and `LEAVE` (when a person exits), which are **TRUE** for one clock period.

The entrance and exit are each narrow enough for only one person to pass through at a time, but it is possible for one person to enter *while* another is exiting during one clock period.

The machine should output an `EMPTY` signal when nobody is in the room and a `FULL` signal when there are 3 people (*the maximum allowed*) in the room. Nobody will be allowed into the room while `FULL` is asserted.

The `EMPTY` and `FULL` signals should be asserted as soon as the conditions are satisfied, i.e. before the next active clock transition.

Derive the state transition diagram. You may assume that an accurate 0.5Hz clock is available as input.